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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/689,599	10/13/2000	Kwang Seop Park	8733.167.00	8223

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EXAMINER	
AKKAPEDDI, PRASAD R	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/689,599	PARK ET AL.	
	Examiner	Art Unit	
	Prasad R Akkapeddi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15-23,27 and 32-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13,15-23,33-42 and 44-60* is/are allowed.

6)☒ Claim(s) *1-12 and 27* is/are rejected.

7)☒ Claim(s) *32 and 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Response to Amendment

2. Applicant's arguments with respect to claims 1-12 and 27 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-12 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. (Gu) (U.S.Patent No. 6,359,672) in view of Shimada et al. (Shimada) (U.S.Patent No. 6,147,722).

a. As to claim 1: Gu discloses a method of fabricating a liquid crystal display device including a thin film transistor (9) gate line (17) and data line (5) on a transparent substrate, forming the organic insulating film (33) on the transparent substrate to a thickness of between 0.9 to 2.75 micrometers (Col. 8, lines 21). This range of thickness overlaps the recited feature in the instant claim. Gu also discloses that the pixel electrode (3) (Col. 5, line 46) and the organic insulating film (33) so as to be overlapped by a predetermined area (Fig. 1) with the gate line (Col. 8, lines 49-51).

Gu also discloses that the organic insulating film (33) is over the address (data) lines (5) (col. 8, lines 14-15).

Also, for overlap of ranges, see MPEP 2131.03 for case law pertaining to rejections based on the anticipation of ranges. Note that the range for the thickness of the organic insulating film of between 0.9 to 2.75 micrometers as disclosed by Gu overlaps the range of 0.8 and 1.5 microns (as asserted in claim 1). Therefore, the range in claim 1 would have at least been obvious. See **In re Malagari**, 499 F.2d 197, 182 USPQ 549 (CCPA 1974).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the Gu LCD device with

the thickness of between 0.8 and 1.5 microns for reducing the potential voltage swings.

Gu teaches that parasitic capacitance is created at overlapped areas (col. 2, lines 7-21) and also teaches the relationship between the parasitic capacitance and the thickness of the layer, dielectric constant and the area of the overlap (col. 5, lines 45-61). However, Gu does not teach that the parasitic capacitance in an overlapping area between the pixel electrode and the data line is different from a parasitic capacitance in an overlapping area between the pixel electrode and the gate line. The overlapped areas as taught by Gu are similar and hence the parasitic capacitance is the same between the areas of overlap of the pixel electrode with either the data line or the gate line.

Shimada on the other hand, discloses different overlapped widths of the pixel electrodes with the gate and data lines (Fig. 3A) and (col. 12, lines 1-52). Hence, if one takes into consideration the different widths for the overlapped areas as taught by Shimada and calculates the parasitic capacitance form the equation of Gu (col. 5, line 55), one can easily get that the parasitic capacitance in an overlapping area between the pixel electrode and the data line is different from a parasitic capacitance in an overlapping area between the pixel electrode and the gate line.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have different parasitic capacitances at the overlapped areas as taught by Shimada to achieve excellent display

characteristics and high aperture ratio devices (col. 1, lines 10-12 and col. 2, lines 46-50).

b. As to claim 7: Gu discloses a liquid crystal display device (Fig. 1) containing a thin film transistor (9) gate line (17) and data line (5) on a transparent substrate, forming the organic insulating film (33) on the transparent substrate to a thickness of between 0.9 to 2.75 micrometers (Col. 8, lines 21). This range of thickness overlaps the recited feature in the instant claim. Gu also discloses that the pixel electrode (3) (Col. 5, line 46) and the organic insulating film (33) so as to be overlapped by a predetermined area (Fig. 1) with the data line (Col. 8, lines 14-15 and lines 49-51), and the source electrode (15) is connected to the pixel electrode (3) (Col.6, lines 32-33). Gu does disclose that the organic insulating film (33) is over the address (data) lines (5) (col. 8, lines 14-15).

Also, for overlap of ranges, see MPEP 2131.03 for case law pertaining to rejections based on the anticipation of ranges. Note that the range for the thickness of the organic insulating film between 0.9 to 2.75 microns as disclosed by Gu, overlaps the range of 0.8 and 1.5 microns as asserted in claim 7.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the Gu LCD device with the thickness of the organic insulating film between 0.8 and 1.5 microns for reducing potential voltage swings (abstract).

Gu teaches that parasitic capacitance is created at overlapped areas (col. 2, lines 7-21) and also teaches the relationship between the parasitic capacitance and the thickness of the layer, dielectric constant and the area of the overlap (col. 5, lines 45-61). However, Gu does not teach that the parasitic capacitance in an overlapping area between the pixel electrode and the data line is different from a parasitic capacitance in an overlapping area between the pixel electrode and the gate line. The overlapped areas as taught by Gu are similar and hence the parasitic capacitance is the same between the areas of overlap of the pixel electrode with either the data line or the gate line.

Shimada on the other hand, discloses different overlapped widths of the pixel electrodes with the gate and data lines (Fig. 3A) and (col. 12, lines 1-52). Hence, if one takes into consideration the different widths for the overlapped areas as taught by Shimada and calculates the parasitic capacitance form the equation of Gu (col. 5, line 55), one can easily get that the parasitic capacitance in an overlapping area between the pixel electrode and the data line is different from a parasitic capacitance in an overlapping area between the pixel electrode and the gate line.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have different parasitic capacitances at the overlapped areas as taught by Shimada to achieve excellent display characteristics and high aperture ratio devices (col. 1, lines 10-12 and col. 2, lines 46-50).

c. As to claims 2-6: Gu discloses that the thickness of the organic insulating film is 0.9 micrometers which is less than1.3 micrometers, and the dielectric constant is about 2.7 (Col. 7, line 37), which is less than 3.0, and the organic insulating film is made from Benzocyclobutene (BCB) (Col. 7, line 26). Gu also discloses that the line-pixel capacitance (also parasitic capacitance Cpl, Col. 5, line 52) value in areas of overlap is less than 9.0 fF (Col. 9, lines 1- 5), and the width of an overlapping area at which the pixel electrode is overlapped with the data line (5) is between 2-3 micrometers (Col. 8, lines 52-53) which is greater than 1.5 micrometers as recited.

d. As to claims 8-12 and 27: Gu also discloses that the dielectric constant is about 2.7 (Col. 7, line 37), which is less than 3.0, and the organic insulating film is made from Benzocyclobutene (BCB) (Col. 7, line 26), the thickness being 0.9 micrometers which is less than 1.3 micrometers. Gu also discloses that the line-pixel capacitance (also parasitic capacitance Cpl, Col. 5, line 52) value in areas of overlap is less than 9.0 fF (Col. 9, lines 1- 5). Also, for overlap of ranges, see MPEP 2131.03 for case law pertaining to rejections based on the anticipation of ranges. Note that the range for the parasitic capacitance value as disclosed by Gu overlaps the range of less than 0.0003pF (asserted in claims 12). Therefore, the range in claims 12 would have at least been obvious. See **In re Malagari**, 499 F.2d 197, 182 USPQ 549 (CCPA 1974).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the Gu LCD device with

the parasitic capacitance value of less than 0.0003pF and adjusting thickness of the organic insulating film between 1.25 and 1.27 microns (as asserted in claim 11), for reducing the capacitive cross talk and permit the insulating means to be photoimaged (col. 4, lines 27-29).

Allowable Subject Matter

5. Claims 32 and 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The allowable subject matter being: "the thickness and the dielectric constant of the organic insulating film are selected such that a liquid crystal pixel cell driven with the pixel electrode charges to a voltage which is more than 95% of a video data voltage within ½ of an enabling interval of a control signal that is applied to a gate electrode for defining a channel of the thin film transistor."

6. Claims 13, 15-23, 33-42 and 44-60 are allowed.

The allowable subject matter being: "the thickness and the dielectric constant of the organic insulating film are selected such that a liquid crystal pixel cell driven with the pixel electrode charges to a voltage which is more than 95% of a video data voltage within ½ of an enabling interval of a control signal that is applied to a gate electrode for defining a channel of the thin film transistor."

Response to Arguments

7. Following is the response by the examiner to the applicant's arguments:

a. Applicant's argument No. 1 (Page 14, lines 13-18 of the remarks dated 10/12/2004): The equation used in Gu et al. is silent as to any relationship between the widths of overlapping areas. Thus, without more information (i.e., the length of overlapping areas), one cannot easily get that the parasitic capacitance in an overlapping area between the pixel electrode and the data line is different from a parasitic capacitance in an overlapping area between the pixel electrode and the gate line.

Examiner's response to argument No. 1: As pointed out earlier, Gu's teaching apply to overlapped areas (sol. 5, lines 45-60) so does the recited limitations in the instant claims. Hence, the argument that Gu's teaching is silent about width and length is not relevant. An area is a product of width and length. The instant claims are also silent about widths and lengths of the overlapped areas. Hence, the teachings of Gu and Shimada as they apply to overlapped areas are still applicable and the argument is moot.

b. Applicant's argument No. 2 (page 15, lines 3-25): ..... Shimada obtains excellent display characteristics as a result of preventing light leakage within reverse tilt domains and 'the proffered motivation is insufficient to establish prima facie case of obviousness as the advantages of Shimada et al. would not be transferred to Gu et al.

Examiner's response to argument No. 2: In response to applicant's argument as described above, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Besides, Shimada explicitly teaches that reverse tilt domains (154) are formed within the overlap portion of the pixel electrode (140) on the gate signal line (104) or the source signal line (102) (col. 13, lines 40) and the excellent display characteristics is obtained by maintaining a high aperture ratio (col. 13, lines 41-48).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prasad R Akkapeddi whose telephone number is 571-272-2285. The examiner can normally be reached on 7:00AM to 5:30PM M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prasad R Akkapeddi, Ph.D
Examiner
Art Unit 2871

PRA

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TARIFUR R. CHOWDHURY
PRIMARY EXAMINER